IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Fang et al.**	Art Unit: 2891
Serial No.: 10/762,445	Examiner: Sarkar, Asok K.
Filed: January 22, 2004	
For: **Structure and Method for Low VSS Resistance and Reduced DIBL in a Floating Gate Memory Cell**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1, 2, 4-9 and 11-14. The Final Rejection issued on October 25, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on January 24, 2006.

REAL PARTY IN INTEREST

The real party in interest is Spansion LLC.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1, 2, 4-9 and 11-14 are pending, and claims 3, 10, and 15-20 were canceled in previous amendments. Claims 1, 2, 4-9 and 11-14 have been finally rejected in a Final Rejection dated October 25, 2005. This Appeal is directed to the rejection of claims 1, 2, 4-9 and 11-14. Claims 1, 2, 4-9 and 11-14 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments have been entered after issuance of the Final Rejection of October 25, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 defines a floating gate memory cell (e.g., floating gate memory cell 202 in Figure 2C) situated on a substrate (e.g., substrate 204 in Figure 2C). The floating gate memory cell (e.g., floating gate memory cell 202 in Figure 2C) includes a stacked gate structure (e.g., stacked gate structure 208 in Figure 2C) situated on the substrate (e.g., substrate 204 in Figure 2C), such that the stacked gate structure is situated over a channel region (e.g., channel region 222 in Figure 2C) in the substrate. A recess (e.g., recess 228 in Figure 2C) having a sidewall (e.g., sidewall 230 in Figure 2C), a bottom (e.g., bottom 232 in Figure 2C), and a depth (e.g., depth 236 in Figure 2C) is formed in the substrate (e.g., substrate 204 in Figure 2C) adjacent to the stacked gate structure (e.g., stacked gate structure 208 in Figure 2C).

The floating gate memory cell (e.g., floating gate memory cell 202 in Figure 2C) further includes a source (e.g., source 234 in Figure 2C) situated adjacent to the sidewall (e.g., sidewall 230 in Figure 2C) of the recess (e.g., recess 228 in Figure 2C) and under the stacked gate structure (e.g., stacked gate structure 208 in Figure 2C). A Vss connection region (Vss connection region 238 in Figure 2C), which is a heavily doped region to reduce a Vss resistance, is situated under the bottom (e.g., bottom 232 in Figure 2C) of the recess (e.g., recess 228 in Figure 2C) and under the source (e.g., source 234 in Figure 2C), such that the Vss connection region is connected to the source. *See*, e.g., page 11, lines 6-7 and Figure 2C of the present application. Thus, the Vss connection

region (Vss connection region 238 in Figure 2C) being situated under the bottom (e.g., bottom 232 in Figure 2C) of the recess (e.g., recess 228 in Figure 2C) advantageously causes the source (e.g., source 234 in Figure 2C) to have a reduced lateral diffusion in the channel region (e.g., channel region 222 in Figure 2C), thereby preventing an increase in a drain induced barrier lowering. *See*, e.g., page 11, lines 15-19 and Figure 2C of the present application.

B. Claim 8

Independent claim 8 defines a floating gate memory cell substantially similar to that defined by independent claim 1.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 2, 4-6, 8, 9, and 11-13 under 35 USC §102(b) as being anticipated by U.S. Patent No. 6,147,379 to Hori et al. (hereinafter "Hori") in view of U.S. Patent No. 6,721,205 to Kobayashi et al. (hereinafter "Kobayashi").

B. Claims 7 and 14 under 35 USC §103(a) as being unpatentable over Hori in view of Kobayashi.

ARGUMENT

A. Rejection of claims 1, 2, 4-6, 8, 9, and 11-13 under 35 USC §102(b) as being anticipated by Hori in view of Kobayashi.

Appellants respectfully submit that the present invention, as defined by independent claims 1 and 8, is patentably distinguishable over Hori and Kobayashi, either singly or in combination.

The Examiner has rejected claims 1, 2, 4-6, 8, 9, and 11-13 under 35 USC § 102(b) as being anticipated by Hori "in view of" Kobayashi. The Examiner has separately rejected claims 7 and 14 under 35 USC § 103(a) as being unpatentable over Hori in view of Kobayashi. For the following reasons, Appellants respectfully submit that the pending claims are patentably distinguishable over the cited art.

In contrast to the present invention, Hori is directed to increasing electron injection efficiency in performing write operations, improving erase operations when taking out electrons from the floating gate into the drain region, suppressing the injection of holes into the oxide film when data is erased, increasing read current, and suppressing the degradation of the read disturb margin. *See*, e.g., column 7, lines 5 through 20 of Hori. However, among its long list of goals and achievements, Hori does not mention a word about lowering ground resistance (or Vss resistance) in the memory array. Nor does Hori mention a word about the harmful DIBL effects, to which the present invention is directed. Thus, Hori does not teach, disclose, or even suggest the advantageous structure

disclosed and claimed by the present invention, nor does Hori achieve the advantages of the present invention embodied in independent claims 1 and 8.

Appellants note that the Examiner has acknowledged that Hori does not address lowering ground resistance (i.e. lowering Vss resistance) in the source region, since the Examiner has relied on Kobayashi as teaching "that Vss connection region is the source of the memory cell through which the reference voltage is applied during the operation of the memory cell in column 19, lines 49-63." Page 3 of the Final Office Action dated October 25, 2005, second paragraph. However, the Examiner has relied on a purported combination of Hori and Kobayashi under 35 USC § 102(b). Appellants submit that 35 USC § 102(b) cannot be used to reject a claim when a combination of two references, instead of a single reference, is relied upon. Assuming that the Examiner mistakenly cited 35 USC § 102(b) while intending to cite 35 USC § 103(a), the Examiner has not provided any arguments why and how the two references, i.e. Hori and Kobayashi, could be combined to achieve the present invention. Appellants submit that Kobayashi is directed to the operation of a memory device without any reference as to a need to reduce DIBL, or the need to reduce the ground resistance, or the need to reduce DIBL while also achieving a reduced ground resistance.

Therefore, Kobayashi cannot be combined with Hori, since there is no motivation or suggestion in Kobayashi (or in Hori) to combine one with the other to achieve the present invention. Thus, since the Examiner has acknowledged that Hori does not

address lowering ground resistance (i.e. lowering Vss resistance) in the source region, Hori lacks a key feature of the present invention.

As noted in Appellants' response to the previous Non-Final Office Action of July 5, 2005, in describing its Figure 1A (the Figure to which the Examiner has referred), Hori acknowledges that: "The nonvolatile semiconductor memory device shown in FIGS. 1A and 1B is principally characterized in (1) that the drain region 8 has a triple structure consisting of the high-concentration drain region 8a, the low-concentration drain region 8b and the extremely-low-concentration drain region 8c, (2) that the low-concentration drain region 8b is formed so as to cover the corner portion at the bottom of the step, (3) that the extremely-low-concentration drain region 8c is formed in the step side region 13 and (4) that the steps have been formed in accordance with an epitaxial growth." Column 11, lines 5-14 of Hori.

Thus, in achieving its write/erase objectives discussed above, Hori focuses on the configuration of the drain region used for writing and erasing data (and not the source region used for providing a ground connection). In this regard, Hori states:

"Since this device has such a drain structure, when a voltage of about 5 V is applied to the drain region 8 in writing data, the extremely-low-concentration drain region 8c is depleted. In this case, since the low-concentration drain region 8b has a higher impurity concentration than that of the extremely-low-concentration drain region 8c, only a part of the low-concentration drain region 8b (i.e., a part adjacent to the extremely-low-

concentration drain region 8c) is depleted. As a result, a high electric field is formed in the corner portion between the second surface region 12 and the step side region 13 . . . ." Column 11, lines 15-25 of Hori. Thus, Hori in fact teaches away from reducing the DIBL problem which requires a lowering of, and not increasing, the electric field adjacent to the drain.

With reference to Figure 1A, Hori does state that: "The source region 7 formed in the first surface region 11 and the third surface region 14 includes a high-concentration impurity layer 7a and a low-concentration impurity layer 7b having an impurity concentration lower than that of the high-concentration impurity layer 7a." Hori, column 9, line 64 through column 10, line 1. However, as clearly shown in Figure 1B (which is the top view of Figure 1A), the region covered by layer 7a includes the "relatively high level (a first surface region 11)" (See Hori, column 8, lines 50-51). In other words, a substantial portion of Hori's "Vss connection region" is at the same elevation level as Hori's "source 7b." Therefore, in Hori, the Vss connection region is not under the source region, as required by the present invention. Thus, not only Hori fails to address the goals of the present invention, but also the invention's structure, as claimed by independent claims 1 and 8, is patentably distinguishable over Hori's disclosed structure.

In "Response to Arguments," the Examiner has stated that Appellants' "arguments are not persuasive for the reason that the Applicant's claim limitations do not specify the position level of the Vss connection region with respect to the source region." Page 5, paragraph 7 of the Final Office Action of October 25, 2005. Appellants respectfully

disagree and submit that both independent claims 1 and 8 clearly point out that the Vss connection region is "situated under said bottom of said recess and under said source." As such, the "position level" of the Vss connection region of the present invention is distinctly defined and pointed out by the independent claims of the present application.

Further, in "Response to Arguments," the Examiner has also stated that: "Although, it is possible that Hori's device will not completely eliminate drain induced barrier lowering it will certainly lower it from the highest level developed without the presence of the heavily doped Vss region." Page 6, lines 2-5 of the Final Office Action of October 25, 2005. However, as discussed in the present application, according to the presently disclosed and claimed invention, it is not merely the presence of the heavily doped Vss connection region, but it is the position of the heavily doped Vss connection regions, i.e. its position as being fully recessed in relation to the source region, that will reduce the DIBL.

For the foregoing reasons, Appellants respectfully submit that the present invention, as defined by independent claims 1 and 8, are patentably distinguishable over Hori and Kobayashi, either singly or in combination. Thus, claims 2 and 4-6 depending from independent claim 1 and claims 9 and 11-13 depending from independent claim 8 are, *a fortiori*, also patentably distinguishable over Hori and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejection of claims 7 and 14 under 35 USC §103(a) as being unpatentable over Hori in view of Kobayashi.

As discussed above, the present invention as defined by independent claims 1 and 8 is patentably distinguishable over Hori and Kobayashi, either singly or in combination. Thus, claim 7 depending from independent claim 1 and claim 13 depending from independent claim 8 are, *a fortiori*, also patentably distinguishable over Hori and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 8 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 2, 4-9, and 11-14 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 2, 4-9, and 11-14 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 3/31/06

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Christina Carter 3/31/06
Signature Date

APPENDIX OF CLAIMS ON APPEAL

Claim 1: A floating gate memory cell situated on a substrate, said floating gate memory cell comprising:

a stacked gate structure situated on said substrate, said stacked gate structure being situated over a channel region in said substrate;

a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth;

a source of said floating gate memory cell situated adjacent to said sidewall of said recess and under said stacked gate structure;

a Vss connection region situated under said bottom of said recess and under said source, said Vss connection region being connected to said source, said Vss connection region being a heavily doped region to reduce a Vss resistance;

wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region, thereby preventing an increase in a drain induced barrier lowering.

Claim 2: The floating gate memory cell of claim 1 wherein said reduced lateral diffusion of said source causes a reduction in drain induced barrier lowering in said floating gate memory cell.

Claim 4: The floating gate memory cell of claim 1 wherein said sidewall of said recess is substantially perpendicular to a top surface of said substrate.

Claim 5: The floating gate memory cell of claim 1 wherein said depth of said recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms.

Claim 6: The floating gate memory cell of claim 1 wherein said stacked gate structure comprises an ONO stack situated on a floating gate.

Claim 7: The floating gate memory cell of claim 1 wherein said floating gate memory cell is a NOR-type floating gate flash memory cell.

Claim 8: A floating gate memory cell situated on a substrate, said floating gate memory cell comprising a stacked gate structure situated on said substrate, said stacked gate structure being situated over a channel region in said substrate, a recess formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth, said floating gate memory cell being characterized in that:

a source of said floating gate memory cell is situated adjacent to said sidewall of said recess and under said stacked gate structure, a Vss connection region is situated under said bottom of said recess and under said source, said Vss connection region being

connected to said source, said Vss connection region being a heavily doped region to reduce a Vss resistance, wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region, thereby preventing an increase in a drain induced barrier lowering.

Claim 9: The floating gate memory cell of claim 8 wherein said reduced lateral diffusion of said source causes a reduction in drain induced barrier lowering in said floating gate memory cell.

Claim 11: The floating gate memory cell of claim 8 wherein said sidewall of said recess is substantially perpendicular to a top surface of said substrate.

Claim 12: The floating gate memory cell of claim 8 wherein said depth of said recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms.

Claim 13: The floating gate memory cell of claim 8 wherein said stacked gate structure comprises an ONO stack situated on a floating gate.

Claim 14: The floating gate memory cell of claim 8 wherein said floating gate memory cell is a NOR-type floating gate flash memory cell.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)